REMARKS

Claims 1-13 are allowed.

Added new Claims 36-54 are Claims 14-34 rewritten in allowable form as suggested by the Examiner to capture allowable material in Claims 16-17, 20, 23-24, 27, 30-31 and 35.

Claims 14-54 are pending.

Claims 14-15, 18-19, 21-22, 25-26, 28-29, 32-33 and 35 are rejected.

I. REJECTION UNDER 35 U.S.C. § 102

According to the M.P.E.P. § 2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d. 1051, 1053 (Fed. Cir. 1987).

The Examiner rejected Claims 14-15, 18,-19, 21-22, 25-26, 28-29, 32-33, and 35 under *35 U.S.C. § 102(a)* as being anticipated by U.S. Patent No. 6,701,464 to *Austen et al.* ("hereinafter *Austen*").

Claim 14 is directed to a method for managing dynamic resource reassignment within a system comprising two steps. In step 1, first missing resources that are missing because of reassignment within the system are determined. In step 2, a missing resource List is updated by deleting any of the first missing resources of step 1 which are included in the missing resource List. The Examiner states that *Austen* discloses step 1 of Claim 14 and cites *Austen* column 1, lines 40-47. The invention of *Austen* is directed to a method and system for reporting error logs within a logical partition (LPAR) environment. Claim 14 is directed to managing dynamic resource reassignment. The cited reference of *Austen* relates only to error logs and how they relate to multiple logical

partitions. *Austen* discloses a method and system for reporting errors in an LPAR computer that ensures error logs are not deleted before each LPAR has had a chance to read them. See *Austen*, column 1, lines 51-54. The disclosure of *Austen* has nothing to do with missing resources or managing resource reassignment within an LPAR. Resources are elements used by the LPARs, for example, devices coupled to an I/O adapter. Nowhere does *Austen* disclose anything relative to resources, *Austen* discloses only steps relative to the deletion or retention of error logs.

The Examiner states that *Austen* discloses step 2 of Claim 14 and cites *Austen*, column 2, lines 29-24. In this recitation, *Austen* states; "when the event scan routine reports 'unread' error logs in the error log partition 18 to the operating system, the event scan routine marks the particular error log as 'read and ready for deletion.' On a periodic basis, the CSP 14 deletes the error logs marked as 'read and ready for deletion' to free space for new log errors." The Applicants fail to see any reference to missing resources, managing resource reassignment or a missing resource List which are recited in Claim 14. The Applicants assert that the Examiner has failed to make a *prima facie* case of anticipation regarding Claim 14 for failing to identify any of the elements of Claim 14 within the cited reference. Therefore, the Applicants assert that the rejection of Claim 14 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above argument.

Claim 15 is dependent from Claim 14 and contains all the limitations of Claim 14. Claim 15 adds the limitation wherein the determining step comprises tagging the first missing resources in a system error log which are missing because of reassignment. The Examiner states that *Austen* discloses the limitation of Claim 15 and cites *Austen* column 2, lines 29-34. The Applicants have shown that *Austen* does not mention missing resources, managing resource reassignment or a missing resource List, nor does *Austen* mention tagging the first missing resources in an error log which are missing because of reassignment. The Applicants assert that the Examiner has failed to make a *prima facie* case of anticipation regarding Claim 15 for failing to identify any of the elements of

Claim 15 within the cited reference. Therefore, the Applicants assert that the rejection of Claim 15 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 14.

Claim 18 is dependent from Claim 14 and contains all the limitations of Claim 14. Claim 18 adds the limitation that the dynamic resource reassignment occurs between logical partitions (LPARs) of the system. The Examiner states that *Austen* discloses Claim 18 and cites *Austen*, column 2, lines 10-12. In this recitation, *Austen* states "FIG. 1 is a block diagram illustrating a logical partition (LPAR) computer system having enhanced error log reporting capability in accordance with the present invention." Again the Applicants do not see any reference to dynamic resource reassignment between LPARs of the system as recited in Claim 18. The Applicants assert that the Examiner has failed to make a *prima facie* case of anticipation regarding Claim 18 for failing to identify any of the elements of Claim 18 within the cited reference. Therefore, the Applicants assert that the rejection of Claim 18 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 14.

Claim 19 is dependent from Claim 15 and contains all the limitations of Claim 15. Claim 18 adds the limitation that the missing resources are tagged in response to reassignment from a first one of the LPARs of the system to a second one of the LPARs of the system. The Examiner states that *Austen* discloses Claim 19 and cites *Austen*, column 2, lines 10-13. In this recitation, *Austen* states "FIG. 1 is a block diagram illustrating a logical partition (LPAR) computer system having enhanced error log reporting capability in accordance with the present invention. The system 10 includes multiple logical partitions 12, a control service processor 14, and a nonvolatile random access memory (NVRAM) 16." Again the Applicants do not see any reference to missing resources tagged in response to reassignment as recited in Claim 19. The Applicants assert that the Examiner has failed to make a *prima facie* case of anticipation regarding Claim 19 for failing to identify any of the elements of Claim 19 within the cited

reference. Therefore, the Applicants assert that the rejection of Claim 19 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 15.

Claim 21 is directed to a computer program product implementing the method steps of Claim 14. The Examiner rejected Claim 21 for the same reasons as Claim 14. The Applicants have shown that the Examiner has failed to make a *prima facie* case of anticipation relative to Claim 14 and thus has failed to make a *prima facie* case of anticipation relative to Claim 21 for the same reasons. Therefore, the Applicants assert that the rejection of Claim 21 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 14.

Claim 22 is dependent from Claim 21 and adds the same limitation to Claim 21 that Claim 15 adds to Claim 14. The Examiner rejected Claim 21 for the same reasons as Claim 14. The Examiner rejects Claim 22 citing the same reference he cited with regards to Claim 15. The Applicants have shown that the Examiner has failed to make a *prima facie* case of anticipation relative to Claim 15 and thus has failed to make a *prima facie* case of anticipation relative to Claim 22 for the same reasons. Therefore, the Applicants assert that the rejection of Claim 22 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 15.

Claim 25 is dependent from Claim 21 and adds the same limitation to Claim 21 that Claim 18 adds to Claim 14. The Examiner rejected Claim 21 for the same reasons as Claim 14. The Examiner rejects Claim 25 citing the same reference he cited with regards to Claim 18. The Applicants have shown that the Examiner has failed to make a *prima facie* case of anticipation relative to Claim 18 and thus has failed to make a *prima facie* case of anticipation relative to Claim 25 for the same reasons. Therefore, the Applicants assert that the rejection of Claim 25 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 18.

Claim 26 is dependent from Claim 21 and adds the same limitation to Claim 21 that Claim 19 adds to Claim 14. The Examiner rejected Claim 21 for the same reasons as Claim 14. The Examiner rejects Claim 26 citing the same reference he cited with regards to Claim 19. The Applicants have shown that the Examiner has failed to make a *prima facie* case of anticipation relative to Claim 19 and thus has failed to make a *prima facie* case of anticipation relative to Claim 26 for the same reasons. Therefore, the Applicants assert that the rejection of Claim 26 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 19.

Claim 28 is an independent claim directed to a data processing system having circuitry for implementing the steps of Claim 14. The Examiner states that *Austen*, in addition to Claim 14, discloses the CPU recited in Claim 28. The Examiner cites *Austen*, column 3, lines 13-14 as disclosing the CPU of Claim 28. In this recitation, *Austen* states "the hypervisor 22 indicates the read status of a new error log in the PLM 24 by marking the entry as 'unread by my partition' in the records 26 for each active logical partition 12, and by marking entry as 'read by my partition' in the records 26 for each inactive logical partition 12 in step 56." The Examiner states that *Austen* discloses the RAM of Claim 28 and cites *Austen*, column 3, lines 14-15. This recitation does not mention RAM or any form of memory. The Examiner states that *Austen* discloses the ROM of Claim 28 and cites *Austen*, column 2, line 16. In this recitation, *Austen* is describing what is included in an LPAR computer system. While it does mention NVRAM in this section, it does not mention ROM as stated by the Examiner. The Examiner states that *Austen* discloses the I/O adapter and bus system coupling the CPU, RAM and ROM of Claim 28 and cites *Austen*, column 2, lines 20-34. The Applicants can find no mention of an I/O adapter or a bus system in the recitation cited by the Examiner. The Applicants have shown that the Examiner has failed to make a *prima facie* case of anticipation relative to Claim 14. The Applicants have shown that *Austen* does not mention the elements above recited in Claim 28 and the Examiner has failed to point out where *Austen* discloses the circuitry for implementing the steps of Claim 14. Thus, the Applicants assert that the Examiner has failed to make a *prima facie* case of anticipation of Claim 28. Therefore, the Applicants

assert that the rejection of Claim 28 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed by the above reasons and for the same reasons as Claim 14.

The Examiner rejected Claim 29 for the same reasons as Claim 15. The Applicants have shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 15. Therefore, the Applicants assert that the rejection of Claim 29 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed for the same reasons as Claim 15.

The Examiner rejected Claim 32 for the same reasons as Claim 18. The Applicants have shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 18. Therefore, the Applicants assert that the rejection of Claim 32 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed for the same reasons as Claim 18.

The Examiner rejected Claim 33 for the same reasons as Claim 26. Claim 33 adds the same limitation to Claim 29 that Claim 26 adds to Claim 21. The Applicants have shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 21. Therefore, the Applicants assert that the rejection of Claim 33 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed for the same reasons as Claim 26.

The Examiner rejected Claim 35 for the same reasons as Claim 25. Claim 35 is directed to the configuration database as a configuration database for a logical partition (LPAR) within the system. Claim 25 is not directed to a configuration database and the Applicants fail to see how Claim 25 applies to the limitation of Claim 35. The Applicants assert that the Examiner has failed to make a *prima facie* case for anticipation relative to Claim 35 for failing to point out where *Austen* discloses the limitation of Claim 35. Therefore, the Applicants assert that the rejection of Claim 35 under *35 U.S.C. § 102(a)* as being anticipated by *Austen* is traversed for the above reasons.

III. CONCLUSION

The Applicants thank the Examiner for allowing Claims 1-13.

New Claims 36-54 are Claims 14-34 rewritten in allowable form as suggested by the Examiner to capture allowable material in Claims 16-17, 20, 23-24, 27, 30-31 and 35 and as such are in allowable form.

The Applicants have traversed the rejections of Claims 14-15, 18,-19, 21-22, 25-26, 28-29, 32-33, and 35 under *35 U.S.C. § 102(a)* as being anticipated by *Austen.*

The Applicants, therefore, respectfully assert that Claims 1-35 and new Claims 36-54 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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